Statement of Research Interest

My name is Omid Farhanieh. My main research interest is low power Analog, RF and mixed-signal Integrated Circuit Design. I am writing to express my interest in pursuing the PhD in Electronics at Department of Electrical Engineering & Computer Science of York University. I am excited by the prospect of performing research and broadening my knowledge of Integrated Circuit design, and I believe I would make an excellent doctoral candidate. Professor Gafar-Zade and I have discussed about the available PhD position in BioSA research group. As he found me a qualified candidate for this position, supporting my application, he has agreed to be my PhD supervisor should I be accepted.

I am passionate about Analog, RF and mixed-signal Integrated Circuit design. During my B.Sc. in Electronics, I had such a strong desire to analysis and design of electronic circuits that always tried to simulate the analog and digital circuits of reference electronics books by simulation tools such as Cadence, HSpice, PSpice and Proteus; that’s why I was highly motivated to pursue my education on electronics in Master’s degree. After graduation from B.Sc., I passed the University entrance exam for M.Sc. degree successfully and got acceptance from University of Tabriz, one of the top 10 universities in Iran. During my M.Sc., I completed multiple, graduate-level courses in Analog and RF integrated circuit design area. Analog and advanced analog IC design, Integrated data converters design (ADC&DAC), Gm-C filters and Switched-Capacitor circuits, High frequency IC design and Semiconductor technology were my completed courses in my M.Sc. which helped me get familiar with vast research aspects of Analog, RF and mixed-signal IC design.

Because of my good performance in graduate courses, excellent communication skills, profound interest in Integrated Circuit design and quick learning, professor Kouzehkonani, dean of faculty, selected me as an outstanding student to work as research assistant in Zigbee SOC research group at Department of Electrical Engineering of the University of Tabriz. This team consisted of seven Analog and Digital IC design M.Sc. and PhD students under management of Dr. Jafar Sobhi working on designing a “2.4 GHz ZigBee System-On-Chip for sensor node in WSN application”. For this project, each part of the system was purposed for the final thesis project of each member of the team. Data converters for sensor interface, RF front-end of receiver, RF front-end of transmitter, Frequency synthesizer and signal shaping, Base-band processor, analog base-band circuitry were the main blocks of the system.

In my share of this project, as requirements of 2.4 GHz ZigBee transceiver and its OQPSK modulation suggest, I designed a highly linear, high efficiency and low power Up-converter Mixer and Power Amplifier. The designed passive Mixer circuit showed 6 dBm of 1 dB compression point and just 2 mW power consumption by its LO drive circuit. Also the Power Amplifier circuit consumes 12 mW of power with 7.12 dBm of 1 dB compression point and maximum power added efficiency around 37 percent.

During this project, we had a 30-minute meeting every day at the end of working time to relate each other about newly learned important points or discuss about any problems during the circuit design work of each member. Working in this group, besides learning to do my research well in both team-oriented and self-directed environments, I got involved in design of other blocks e.g. LNA and Frequency Synthesizer and gained important experience in design of other blocks.

After graduation from M.Sc., I was extremely determined to get admission from one of the top ranked universities in Europe or North America to continue and focus my research on Analog and RF IC design. My main goal was obtaining a PhD degree with an excellent performance and a number of fabricated ICs with a state of the art research and publications so that I can become one of the distinguished professors in this area in future. Although I had good chances for PhD position at that time, during my applications for PhD position, I was informed that my father is diagnosed with a very malignant cancer; that’s why I decided to start my PhD in Sabanci University, one of the top 5 universities in Turkey, to ease my travels to Iran for visiting him; although, it is been four months now since I lost him.

It is been two years that I am a PhD student at Sabanci University working on design of "Driver IC for a High Intensity Focused Ultrasound (HIFU) catheter ablation system" in Acoustic group. ASIC design for ultrasound transducer front-ends is my responsibility in this project. During this two year period, as well as passing all seven graduate courses, three successfully designed ICs are prosperous results of my PhD research so far. In my first chip I designed a High Voltage driver IC for high intensity focused ultrasound transducer. Generally in Ultrasound Transducers using in noninvasive medical ablation equipments, a high voltage driver circuit with capability of driving heavy loads at high voltage and high output current by high slew rate pulses is the key determinant factor for defining the accuracy of systems. Because of our intravascular type of application, we required to design the HIFU Driver Circuit on a very small chip in less than 4 mm2 chip area. For this purpose we used AMS 0.35 um HV-CMOS technology. As an expert in almost all design, simulation, layout, verification and post-layout simulation tools of Cadence, I designed an eight-channel high voltage class D power amplifier as driver IC with more than 85 percent efficiency, operating in 8-12 MHz range and producing 50 V square wave pulses. This HV driver along with a beamformer digital circuit was my first chip, which I designed in the first year of my PhD. I also published the design of the first chip in IEEE UFFC, presented in 2014 IEEE International Ultrasonics Symposium Chicago, Illinois, USA. I am now waiting for fabrication of the ultrasound transducer by other member of our group to prepare a journal paper from the experimental test results with transducer.

After the first chip, we decided to generate a precise clock reference signal, required for beamformer circuit, inside the chip to reduce pin count of system and increase the accuracy of the final high voltage pulses. For this purpose we should design a Phase Locked Loop frequency synthesizer operating between 128-192 MHz and apply this signal to beamformer to produce 8-12 MHz signals required for input of HV driver. Whole this system, containing the HV driver, Beamformer and PLL was my second designed chip. In my third chip I proposed an innovative idea to design a new PLL, with operation frequency of 8-12 MHz and a new scheme to eliminate the beamformer circuit. By this idea the power consumption of PLL and beamformer decreased about 80 percent and occupied chip area is decreased more than 50 percent compared with the second chip. As the second and third chips were taped out in the same run, moreover, because I have newly finished the measurements, I am now preparing journal paper/s from these chips. In experiment, both PLLs show around -94 dBc/decade phase noise and 65 and 62 degree Phase margin for 10 MHz and 160 MHz PLLs respectively.

All these three chips are designed completely based on my IC design knowledge and with carefully considering the CMOS technology specification documents provided by foundry. As the only IC designer of my group in Sabanci University, all IC foundry related procedures such as tape out order, defining of packaging and wire bonding diagram besides other paperwork are being done by me. I should add that for these three ICs(expect the design of beamformer), all design steps including circuit design, full simulations, layout, DRC, LVS, extraction, post layout simulation, PCB design for chip test and chip measurement are performed by me. I believe I have precious experiences in CMOS Analog, mixed signal and RF IC design steps from a basic idea up to chip test and measurement.

I have also performed the design, layout and post-layout simulation for a high tune range (5.5 GHz), low phase noise (-105 dBc/Hz @1 MHz offset) LC-VCO using SiGe 0.25 um HBT for Ku band during these two years. Considering the low power 2.4 GHz Power amplifier and Mixer blocks of my M.Sc. thesis project in TSMC RF 0.18 um as well as my current three chips in AMS HV CMOS 0.35 um, I have experience of circuit design with different CMOS, HV-CMOS and SiGe BiCMOS technologies.

By designing the mentioned three chips for HIFU catheter, I have almost finished my ASIC design work in this project; considering the project will also be finished by three months totally; Also, our coming project will be completely in acoustic area, thus we won’t have any strong Analog, RF or mixed-signal IC design related project in near future which can conduct my PhD thesis project during the remaining two years of my PhD. On the other hand, although I had a remarkable research and very good performance in Sabanci University, I believe studying at the Sabanci University cannot satisfy my desire for an outstanding research anymore. I feel my thirst to have a state of the art research in my PhD is higher than what Sabanci University can provide for me.

Trying to find the best way to enhance my academic and research situation while perusing the Website of York University which is well known for its eminent faculty members and cutting-edge research facilities and projects, I found a vacant PhD position for an Integrated Circuit designer in BioSA laboratory announced by Dr. Gafar-Zade. After I sent Dr. Ghafar-Zade my resume, he arranged a Skype interview with me; we had about two hours talk when I introduced myself and my research and educational background in details and Dr. Ghafar-Zade discussed about their research at BioSA, the requirements of the mentioned PhD position, outstanding features of York University and possible research chances for me in BioSA.

Talking to Dr. Ghafar-Zade and learning more details about his projects, I am sure that being a PhD student in his exceptional group and studying at York University would provide me with an ideal platform for achieving my goals by a remarkable research. I firmly believe York University, by its commitment to excellence, is going to be one of the most top ranked universities in near future in the world. Of course beside the best faculty members, the million dollars of external research findings and cutting edge research facilities, York University requires the most motivated researchers who are also committed to excellence in their research fields. This unlimited appetite to excellence is also my main reason that motivated me to decide to cut my PhD after two years from Sabanci University and apply for a PhD position in your university.

Dear respected committee members, as you well know, it usually takes one or two semesters for a new PhD student to adapt him/her to disciplines of study and research in PhD degree; but it is now two years that I am a PhD student completely familiar with the responsibilities of a PhD student's. During these two years, while passing seven PhD courses, I have performed the design of three chips beside teaching assistantship for Biomedical Instrumentation and Digital Integrated Circuit Design courses; therefore I am sure that my experiences gained during my PhD till know will help me in any other PhD programs. If it is possible in York University and you also consent, in order to save more time for research, it will be very useful for me to transfer some of my completed courses during my PhD in Sabanci University to your university. As you can see, my application to this position itself shows my highest possible motivation to carry out an excellent PhD degree; because I am really sacrificing two years of my life spent in PhD program of Sabanci University in exchange for gaining a higher research possibilities and to perform a unique PhD research which would be definitely possible in York University. My strong research background can also be seen from one Journal paper published in "Analog Integrated Circuits and Signal Processing", Springer Netherlands, three published conference papers in IEEE and two journal papers, being prepared for submission.

I believe that I Posses the aptitude, discipline and diligence to sustain the motivation and drive needed for a PhD degree. I would be grateful, if I am accorded the opportunity to pursue my PhD studies in your prestigious university. Thank you very much for considering my application.

Yours sincerely,  
Omid Farhanieh